WHAT IS CLAIMED IS:

1. A system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement, said clock synchronizer arrangement for effectuating data transfer between a core clock domain and a bus clock domain wherein said core clock domain is operable with a core clock signal and said bus clock domain is operable with a bus clock signal, said core and bus clock signals having a ratio, comprising:

means disposed in a bus clock synchronizer controller portion for generating a set of inter-controller clock relationship control signals; and

means disposed in a core clock synchronizer controller portion operating responsive to said set of inter-controller clock relationship control signals for synchronizing cycle and sequence information associated with said core clock signal relative to said bus clock signal.

2. The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 1, wherein said means disposed in said bus clock synchronizer controller portion for generating a set of inter-controller clock relationship control signals is operable responsive to a SYNC pulse that is sampled in said bus clock domain by said bus clock signal.

3. The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 2, wherein said SYNC pulse is generated by a phase-locked loop (PLL) when a rising edge in said core clock signal is at least substantially coincident with a rising edge in said bus clock signal.

4. The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 2, wherein said means disposed in said core clock synchronizer controller portion is operable responsive to said SYNC pulse that is sampled in said core clock domain by said core clock signal.

5. The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 4, wherein said set of inter-controller clock relationship control signals includes a control signal indicative of an initial sequence and cycle with respect to said bus clock signal.

6. The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 5, wherein said set of inter-controller clock relationship control signals includes a control signal indicative of a clock frequency ratio associated with said bus clock and core clock signals.

7. The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 6, wherein said set of inter-controller clock relationship control signals includes a control signal that is derived by delaying said sampled SYNC pulse by a number of bus clock cycles.

8. The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 7, wherein said means disposed in said core clock synchronizer controller portion includes a sync_ratio sampling means for sampling said control signal indicative of a clock frequency ratio associated with said bus clock and core clock signals.

9. The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 7, wherein said means disposed in said core clock synchronizer controller portion includes a sequence sampling means for sampling said control signal indicative of an initial sequence and cycle with respect to said bus clock signal.

10. The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 7, wherein said means disposed in said core clock synchronizer controller portion includes a delayed_sync sampling means for sampling said control signal that is derived by delaying said sampled SYNC pulse by a number of bus clock cycles.

11. The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 7, further including means disposed in said core clock synchronizer controller portion for determining that said clock frequency ratio is stable.

12. A method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement, said clock synchronizer arrangement for effectuating data transfer between a core clock domain and a bus clock domain wherein said core clock domain is operable with a core clock signal and said bus clock domain is operable with a bus clock signal, said core and bus clock signals having a ratio, comprising:

generating a set of inter-controller clock relationship control signals in a bus clock synchronizer controller portion; and

responsive to said inter-controller clock relationship control signals, synchronizing cycle and sequence information associated with said core clock signal relative to said bus clock signal in a core clock synchronizer controller portion.

13. The method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 12, wherein said inter-controller clock relationship control signals are generated responsive to a SYNC pulse that is sampled in said bus clock domain by said bus clock signal.

14. The method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 13, wherein said SYNC pulse is generated by a phase-locked loop (PLL) when a rising edge in said core clock signal is at least substantially coincident with a rising edge in said bus clock signal.

15. The method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 13, wherein said operation of synchronizing cycle and sequence information associated with said core clock signal relative to said bus clock signal is performed depending on said SYNC pulse that is sampled in said core clock domain by said core clock signal.

16. The method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 15, wherein said set of inter-controller clock relationship control signals includes a control signal indicative of an initial sequence and cycle with respect to said bus clock signal.

17. The method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 16, wherein said set of inter-controller clock relationship control signals includes a control signal indicative of a clock frequency ratio associated with said bus clock and core clock signals.

18. The method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 17, wherein said set of inter-controller clock relationship control signals includes a control signal that is derived by delaying said sampled SYNC pulse by a number of bus clock cycles.

19. The method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 18, wherein said operation of synchronizing cycle and sequence information associated with said core clock signal relative to said bus clock signal includes sampling said control signal indicative of a clock frequency ratio associated with said bus clock and core clock signals.

20. The method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 18, wherein said operation of synchronizing cycle and sequence information associated with said core clock signal relative to said bus clock signal includes sampling said control signal indicative of an initial sequence and cycle with respect to said bus clock signal.

21. The method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 18, wherein said operation of synchronizing cycle and sequence information associated with said core clock signal relative to said bus clock signal includes sampling said control signal that is derived by delaying said sampled SYNC pulse by a number of bus clock cycles.

22. The method of coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 18, further including determining that said clock frequency ratio is stable for synchronizing cycle and sequence information associated with said core clock signal.

23. A computer system having an apparatus for coordinating synchronizer controllers disposed in a clock synchronizer arrangement, said clock synchronizer arrangement for effectuating data transfer between a core clock domain and a bus clock domain wherein said core clock domain is operable with a core clock signal and said bus clock domain is operable with a bus clock signal, said core and bus clock signals having a ratio, comprising:

a sync counter and a ratio detector operating responsive to a sampled SYNC pulse in said bus clock domain for determining a sync_ratio signal;

a cycle generator operating responsive to said sync_ratio signal and said sampled SYNC pulse in said bus clock domain for generating a cycle information signal indicative of a current bus clock cycle;

a sequence generator operating responsive to said sync_ratio signal and said sampled SYNC pulse in said bus clock domain for generating a sequence signal relative to said current bus clock cycle;

a sync delay block operating responsive to said sync_ratio signal and said sampled SYNC pulse in said bus clock domain for generating a syncb0 signal;

a sync ratio sampler block disposed said core clock domain for sampling said sync_ratio signal;

a sequence sampler block disposed in said core clock domain for sampling said sequence signal;

a delayed_sync sampler block disposed in said core clock domain for sampling said syncb0 signal;

logic circuitry disposed in said core clock domain for determining that said sampled sync_ratio signal has stabilized; and

a cycle and sequence generator block disposed in said core clock domain for generating control signals indicative of cycle and sequence information associated with said core clock signal, said cycle and sequence generator block operating responsive to a sync_redge signal generated by a sync pulse detector in said core clock domain and a plurality of intermediary control signals generated by said sync_ratio sampler, said sequence sampler, said delayed_sync sampler and said logic circuitry, wherein said cycle and sequence information associated with said core clock signal is synchronized relative to said bus clock signal's cycle and sequence information.

24. The computer system as recited in claim 23, wherein said sampled SYNC pulse is generated by sampling a SYNC pulse using said bus clock signal.

25. The computer system as recited in claim 24, wherein said SYNC pulse is generated by a phase-locked loop (PLL) when a rising edge in said core clock signal is at least substantially coincident with a rising edge in said bus clock signal.

26. A system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement, said clock synchronizer arrangement for effectuating data transfer between a core clock domain and a bus clock domain wherein said core clock domain is operable with a core clock signal and said bus clock domain is operable with a bus clock signal, said core and bus clock signals having a ratio, comprising:

means disposed in a core clock synchronizer controller portion for generating a set of inter-controller clock relationship control signals; and

means disposed in a bus clock synchronizer controller portion operating responsive to said set of inter-controller clock relationship control signals for synchronizing cycle and sequence information associated with said bus clock signal relative to said core clock signal.

27. The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 26, wherein said means disposed in said core clock synchronizer controller portion for generating a set of inter-controller clock relationship control signals is operable responsive to a SYNC pulse that is sampled in said core clock domain by said core clock signal.

28. The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 27, wherein said SYNC pulse is generated by a phase-locked loop (PLL) when a rising edge in said core clock signal is at least substantially coincident with a rising edge in said bus clock signal.

29. The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 27, wherein said means disposed in said bus clock synchronizer controller portion is operable responsive to said SYNC pulse that is sampled in said bus clock domain by said bus clock signal.

30. The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 29, wherein said set of inter-controller clock relationship control signals includes a control signal indicative of an initial sequence and cycle with respect to said core clock signal.

31. The system for coordinating synchronizer controllers disposed in a clock synchronizer arrangement as recited in claim 30, wherein said set of inter-controller clock relationship control signals includes a control signal indicative of a clock frequency ratio associated with said bus clock and core clock signals.